

SEMICONDUCTOR DEVICE WITH CONTACTS HAVING UNIFORM CONTACT
RESISTANCE AND METHOD FOR MANUFACTURING THE SAME

5 Related Application

This application relies for priority upon Korean Patent Application No. 2001-8755, filed on February 21, 2001, the contents of which are herein incorporated by reference in their entirety.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and a method for manufacturing the same and the semiconductor device, and more particularly, to a semiconductor device having a contact hole which is capable of maintaining contact resistance of a contact connecting multi-layered interconnections and a method for manufacturing the same.

2. Description of the Related Art

As the integration density of semiconductor devices increases, a multi-layered interconnection structure is required. However, in most cases, an insulating layer on which an interconnection layer will be placed is not flat, and thus contact resistance is not uniform along the entire surface of a semiconductor substrate. This problem will be described with reference to FIG. 1.

Referring to FIG. 1, a transistor (not shown) or a capacitor (not shown) is formed on a semiconductor substrate 10, and a first interlayer insulating layer 12 is formed before an interconnection layer 14 is formed. To planarize the first interlayer insulating layer 12, chemical mechanical polishing (CMP) may be used. Even if the CMP technique is performed on the entire surface of the semiconductor substrate 10, it is very difficult to etch the first interlayer insulating layer 12 to a uniform thickness. In addition, CMP equipment is very expensive.

Thus, in most cases, an interconnection layer 14 and a capping layer 16 are formed on the first interlayer insulating layer 12 that is not planarized. Thus, the thickness of a second interlayer insulating layer 18 formed on the interlayer insulating layer 12 is not uniform.

The interconnection layer 14 is a metal layer containing aluminum. Contact holes 20a, 20b and 20c are formed by etching predetermined portions of the second interlayer insulating layer 18 covering the interconnection layer 14. In this case, oxygen components in the second interlayer insulating layer 18 may diffuse outwardly and then react with aluminum components in the interconnection layer 14 exposed by the contact holes 20a, 20b and 20c. Due to the reaction of oxygen with aluminum, an aluminum oxide layer (not shown), an insulating layer, is formed on the bottom surface of the contact holes 20a, 20b and 20c, that is, the top surface of the interconnection layer 14. To prevent the formation of the aluminum oxide layer, a capping layer 16, which is conductive and can prevent the reaction of oxygen with aluminum is formed on the interconnection layer 14. The capping layer 16 is usually formed of TiN, Ti/TiN, or TaN. Since the capping layer 16 has high resistance, the capping layer 16 is slightly etched to a predetermined depth so that the bottom surface of the contact holes 20a, 20b and 20c is within the capping layer 16.

As described above, the thickness of the second interlayer insulating layer 18 covering the interconnection layer 14 and the capping layer 16 is not uniform along the entire surface of the semiconductor substrate 10. Accordingly, the thickness of the capping layer 16 remaining on the interconnection layer 14 after the etching process for forming the contact holes 20a, 20b, and 20c is not uniform. As a result, the contact resistance of the interconnection layer 14 varies, and thus the speed of information transmission may be different for different regions of the semiconductor device. In other words, the reliability of the semiconductor device may be lowered.

SUMMARY OF THE INVENTION

To solve the above problems, it is a first object of the present invention to provide a semiconductor device having a contact hole by which a uniform contact resistance value can be obtained from any region of the surface of a semiconductor substrate.

It is a second object of the present invention to provide a method for manufacturing a semiconductor device having a contact hole by which a uniform contact resistance value can be obtained from any region of the surface of a semiconductor substrate.

Accordingly, to achieve the first object, there is provided a semiconductor device including a semiconductor substrate; an interconnection layer formed on a portion of the semiconductor substrate; an interlayer insulating layer formed on the entire surface of the interconnection layer of the semiconductor substrate and including a contact hole placed on the interconnection layer; a capping layer formed from the top surface of the interconnection

layer to the bottom surface of the contact hole; an etching stopper formed on the capping layer along the outside walls of the contact hole; and a conductive layer filling the contact hole.

The capping layer may be in contact with the bottom surface and portions of the 5 sidewalls of the contact hole. The interconnection layer is formed of a metal layer containing aluminum. The capping layer is formed of one of TiN, Ti/TiN, and TaN. The conductive layer is formed only in the contact hole, or the conductive layer is an upper interconnection layer filling the contact hole and covering the top surface of the interlayer insulating layer.

To achieve the second object of the present invention, there is provided a method for 10 manufacturing a semiconductor device including sequentially forming an interconnection layer, a capping layer, and an etching stopper on a semiconductor substrate; forming an interlayer insulating layer having a first contact hole exposing a portion of the surface of the etching stopper using a material having a high selectivity with respect to the etching stopper; forming a second contact hole to expose the top surface of the capping layer by removing the 15 etching stopper exposed by the first contact hole; and forming a conductive layer to fill the second contact hole.

The method for manufacturing a semiconductor device further includes forming a 20 third contact hole by slightly etching a portion the capping layer exposed by the second contact hole before forming a conductive layer. Here, the conductive layer fills the second contact hole and the third contact hole. The second and third contact holes are formed by 25 performing a dry etching method using an etchant having a low selectivity between the etching stopper and the capping layer. The interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers for forming the interconnection layer, the capping layer, and the etching stopper, and patterning the material layers by the same etching process.

The interconnection layer is a metal layer containing aluminum. The capping layer is formed of one of TiN, Ti/TiN and TaN. The interlayer insulating layer is formed of one selected from the group consisting of a silicon oxide layer, a silicon nitride layer, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), 30 tetraethylorthosilicate (TEOS), plasma enhanced TEOS (PE-TEOS), and undoped silicate glass (USG).

The conductive layer may be formed only in the second contact hole or may be formed only in the second and third contact holes. Or the conductive layer may be an upper interconnection layer filling the second contact hole and covering the top surface of the

interlayer insulating layer. Or the conductive layer may be an upper interconnection layer filling the second and third contact holes and covering the top surface of the interlayer insulating layer.

It is possible to obtain uniform contact resistance between the lower interconnection layer and the upper interconnection layer from any region of the surface of a semiconductor substrate irrespective of the degree of flatness of an interlayer insulating layer placed under the lower interconnection layer. Therefore, it is possible to prevent the reliability of a semiconductor device from being lowered.

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BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

15 FIG. 1 is a cross-sectional view of a semiconductor device having a conventional contact hole for connecting multi-layered interconnection layers with each other;

20 FIGS. 2, 3, 4A and 4B are cross-sectional views illustrating a method for manufacturing a semiconductor device having a contact hole for connecting multi-layered interconnection layers with each other according to the present invention;

25 FIG. 5A is a diagram illustrating one embodiment of the relationship between a contact hole and a capping layer; and

FIG. 5B is a diagram illustrating another embodiment of the relationship between a contact hole and a capping layer.

DETAILED DESCRIPTION OF THE INVENTION

25 The present invention will now be described more fully with reference to the accompanying drawings in which preferred embodiments of the invention are shown.

Referring to FIG. 2, a transistor (not shown) or a capacitor (not shown) is formed on a semiconductor substrate 50, and then a first interlayer insulating layer 52 is formed before an interconnection layer is formed.

30 A conductive layer for interconnections (not shown), a material layer for capping, (not shown) and a material layer for stopping etching (not shown) are sequentially deposited on the surface of the first interlayer insulating layer 52. The material layer for stopping etching is patterned, and then the material layer for capping and the conductive layer for interconnections are patterned using the patterned material layer for stopping etching. As a

result, interconnection layers 54, capping layers 56a, 56b, and 56c and etching stoppers 58a, 58b, and 58c are sequentially formed. The interconnection layers 54 are a metal layer containing aluminum, and the capping layers 56a, 56b, and 56c are formed of TiN, Ti/TiN or TaN. The etching stoppers 58a, 58b, 58c are formed of a material having a high etching selectivity with respect to a second interlayer insulating layer 60 which will be formed later, such as an inorganic anti-reflecting layer (ARL) or an organic anti-reflecting coating (ARC) which is typically used in a semiconductor device.

Next, the second interlayer insulating layer 60 is formed over the surface of the first interlayer insulating layer 52 on which the interconnection layers 54, the capping layers 56a, 56b, and 56c and the etching stoppers 58a, 58b, and 58c have been formed. The second interlayer insulating layer 60 is a silicon oxide layer, a silicon nitride layer, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), tetraethylorthosilicate (TEOS), plasma enhanced TEOS (PE-TEOS), or undoped silicate glass (USG). The surface of the second interlayer insulating layer 60, as well as that of the first interlayer insulating layer 52, is not flat. Thus, the thickness of a portion of the second interlayer insulating layer 60 on one of the etching stoppers 58a, 58b, and 58c is different from the thickness of a portion of the second interlayer insulating layer 60 on the others. For example, the portion of the second insulating layer 60 over the etching stopper 58b is thicker than over the etching stoppers 58a and 58c.

Next, predetermined portions of the second interlayer insulating layer 60 are etched by using a dry etching method so that first contact holes 62a, 62b, and 62c are formed. The first contact holes 62a, 62b, and 62c expose the etching stoppers 58a, 58b, and 58c. As described above, the thickness of a portion of the second interlayer insulating layer 60 on one of the etching stoppers 58a, 58b, and 58c is different from the thickness of a portion of the second interlayer insulating layer 60 on the others. In particular, the portion of the second insulating layer 60 over the etching stopper 58b is thicker than over the etching stoppers 58a and 58c. Thus, the portion of the second interlayer insulating layer 60 on the etching stopper 58b (shown in the middle of FIG. 2) should be etched most deeply. Each of the etching stoppers 58a, 58b, and 58c is formed of a material having a high etching selectivity with respect to the interlayer insulating layer 60. Accordingly, even if an etching process is further performed on the second insulating layer 60 remaining on etching stopper 58b (not shown) after the first contact holes 62a, 62b and 62c are formed, the etching stoppers 58a and 58c exposed by the contact holes 62a and 62c, respectively, will hardly be etched.

Referring to FIG. 3, the exposed etching stoppers 58a, 58b, and 58c and portions of the capping layers 56a, 56b, and 56c are removed so that second contact holes 64a, 64b, and 64c are formed. The second contact holes 64a, 64b, and 64c are formed by performing a dry etching method using an etchant having a low etching selectivity between the etching
5 stoppers 58a, 58b, 58c and the capping layers 56a, 56b, and 56c. The bottom surfaces of the first contact holes 62a, 62b and 62c were the top surfaces of the etching stoppers 58a, 58b, and 58c in FIG. 2. In forming the second contact holes 64a, 64b, and 64c, the etching
10 stoppers 58a, 58b, and 58c of FIG. 2 are etched through, and the capping layers 56a, 56b, and 56c of FIG. 2 are etched to a uniform thickness over the surface of the semiconductor
15 substrate. As a result, after the second contact holes 64a, 64b, and 64c are formed, capping
20 layers 56a', 56b', and 56c' are formed to have a uniform thickness, and thus the contact
resistance of the interconnection layers 54 is substantially uniform.

Subsequently, a conductive layer is formed over the surface of the second interlayer
5 insulating layer 60 including the second contact holes 64a, 64b and 64c to fill the second
contact holes 64a, 64b and 64c. The conductive layer may be formed of aluminum or
25 tungsten. FIG. 4A illustrates an upper interconnection layer 66 which is formed by filling the second contact holes 64a, 64b and 64c and covering the top surface of the second interlayer
30 insulating layer 60 with the above-mentioned conductive layer. On the other hand, FIG. 4B
35 illustrates landing plugs 68a, 68b and 68c formed by just filling the contact holes 64a, 64b
40 and 64c with the conductive layer.

FIG. 5A is a diagram showing in more detail the etching stopper 58b' and the capping
layer 56b'. The portion indicated by reference numeral 80 associated with the second contact
hole 64b includes the etching stopper 58b', the capping layer 56b', and the interconnection
layer 54. Alternatively, the bottom surfaces of the second contact holes 64a, 64b, and 64c
25 can be the top surfaces of the capping layers 56a, 56b, and 56c as illustrated in FIG. 5B.

According to the present invention, it is possible for the bottom surface of a contact
hole for connecting a lower interconnection layer to an upper interconnection layer to be at
the top surface of a capping layer on the lower interconnection layer or in the capping layer,
irrespective of topology of the lower interconnection layer or the degree of flatness of an
30 interlayer insulating layer covering the lower interconnection layer. Therefore, it is possible
to obtain a uniform contact resistance value from any region of the surface of a
semiconductor substrate.

While this invention has been particularly shown and described with reference to
preferred embodiments thereof, it will be understood by those skilled in the art that various

changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

Patent Application
MJM Do. No. 9898-188